**MONDAY 14 NOVEMBER 2011**

09.00 Opening and welcome  
*Viktor Öwall, Lund University (SE)*

09.15 Invited talk: Efficiency and flexibility  
*Dejan Marković, University of California LA (US)*

10.00 IR-UWB Technology on Next Generation RFID Systems  
*Kin Keung Lee et al, University of Oslo (NO)*

10.20 Transistor Sizing for a 4-State Current Mode Analog Channel Decoder in 65-nm CMOS  
*Reza Meraji, Lund University (SE)*

10.40 Coffee

1.1 ANALOG TO DIGITAL CONVERTERS  
CHAIR: ERIK BRUUN, TECHNICAL UNIVERSITY OF DENMARK (DK)

11.10 10 GS/s 8-bit Bipolar THA in SiGe Technology  
*Yevgen Borokhovych et al, IHP (DE)*

11.30 Charge Scaling 10-bit Successive Approximation A/D Converter with Reduced Input Capacitance  
*Olli Kursu et al, Oulu University (FI)*

11.50 A Continuous Time Delta Sigma Modulator with Reduced Clock Jitter Sensitivity through DSCR Feedback  
*Dejan Radjen et al, Lund University (SE)*

1.2 DIGITAL HARDWARE FOR SIGNAL PROCESSING AND COMMUNICATION  
CHAIR: VIKTOR ÖWALL, LUND UNIVERSITY (SE)

11.10 Implementation of Narrow-Band Frequency-Response Masking for Efficient Narrow Transition Band FIR Filters on FPGAs  
*Syed Asad Alam et al, Linköping University (SE)*

11.30 On Hardware Implementation of Radix 3 and Radix 5 FFT Kernels for LTE systems  
*Johan LÖFGREN et al, Lund University (SE)*

11.50 Complexity analysis of IOTA filter architectures in Faster-than-Nyquist multicarrier systems  
*Deepak Dasalukunte et al, Lund University (SE)*

12.10 Lunch

13.30 Invited talk: SAW-less Software-Defined Radio Transceivers in 40nm CMOS  
*Jan Craninckx, IMEC (BE)*

2.1 RF POWER AMPLIFIERS  
CHAIR: HENRIK SJÖLAND, LUND UNIVERSITY (SE)

14.15 On Wafer X-Parameter Based Modeling of a Switching Cascode Power Amplifier  
*Yelin Wang et al, Aalborg University (DK)*

14.35 Wideband Limit Study of a GaN Power Amplifier Using Two-Tone Measurements  
*Felice TAFURI et al, Aalborg University (DK)*
2.2 ARITHMETIC CIRCUITS
CHAIR: PEETER ELLERVEE, TALLINN UNIV. OF TECHNOLOGY (EE)

14.15 A Ternary Adiabatic Logic (TAL) Implementation of a Four-Trit Full-Adder
David J Willingham et al, University of Westminster (UK)

14.35 Magnitude Scaling for Increased SFDR in DDFS
Petter Källström et al, Linköping University (SE)

3. POSTER SESSION I
14.55 Coffee / Poster session:
A 2.7–6.1GHz CMOS Local Oscillator Based on Frequency Multiplication by 3/2
Andrea Bevilacqua et al, Lund University (SE)

Very High Bandwidth Semi-Digital PLL with Large Operating Frequency Range
Puneet Sareen et al, Linköping University (SE)

Modeling of Cascode Modulated Power Amplifiers
Daniel Sira et al, Aalborg University (DK)

A Low Voltage Low Power CMOS Analog Multiplier
Amir Miremadi et al, Islamic Azad University (IR)

An empirical study of the stability of 4th-order Incremental-Sigma-Delta-ADCs
Johannes Uhlig et al, Technische Universität Dresden (DE)

Techniques, Problems and Solutions in Designing Multi-GHz All Digital Phase Locked Loops
Muhammad Shakir et al, Lund University (SE)

Comparison of time-varying and non-time-varying Volterra analysis for finding distortion contributions in mixers
Timo Rahkonen et al, University of Oulu (FI)

Comparison and IIP2 Analysis of Two Wideband Balun-LNAs Designed in 65nm COMS
Lin Zhu et al, Lund University (SE)

Use of a Calibrated Voltage Reference to Enhance the Performance of Switched Capacitor Sigma-Delta ADCs over Process Corner
Ronald Spilka et al, Johannes Kepler University (AT)

Dynamic Bias Scheme for Class-C VCO
Luca Fanori et al, Lund University (SE)

An Improved Common-Mode Feedback Loop for the Differential-Difference Amplifier
Andrea Simonetti et al, University of Rome (IT)

4.1 ELECTRONIC DEVICES
CHAIR: MARKKU ÅBERG, VTT (FI)

16.00 Electrical Properties of CVD-Graphene FETs
Johanna Anteroinen et al, Aalto University (FI)

16.20 Adaptive Photovoltaic Cell Simulation with Maximum Power Point Tracking Simulation for Accurate Energy Predictions
Christian Schuss et al, University of Oulu (FI)

16.40 A 85dB Dynamic Range Transimpedance Amplifier in 40nm CMOS Technology
Mohammed Farag Hassan et al, ????

4.2 NETWORK-ON-CHIP
CHAIR: ALBERTO NANNARELLI, TECHNICAL UNIVERSITY OF DENMARK (DK)

16.00 Contention aware scheduling for NoC-based real-time systems
Mihkel Tagel et al, Tallinn University of Technology (EE)

16.20 A Fault-Tolerant and Hierarchical Routing Algorithm for NoC Architectures
Mojtaba Valinataj Babol University of Technology (IR)

16.40 An Adaptive Router Architecture for Heterogeneous 3D Networks-on-Chip
Michael Opoku Agyeman et al, Glasgow Caledonian University (UK)

17.00 The European Spallation Source – ESS
David McGinnis, ESS

18.30 Bus departure to restaurant

19.00 Dinner
5.1 Sub-Harmonic Mixers
CHAIR: PIETRO ANDREANI, LUND UNIVERSITY (SE)

09.45 A Divide-by-Three Regenerative Frequency Divider Using a Subharmonic Mixer
Brad Jackson et al, Queen’s University (CA)

10.05 Injection-Locked Superharmonic Self-Oscillating Mixer
Tero Koivisto et al, University of Turku (FI)

5.2 Processors
CHAIR: JOACHIM RODRIGUES, LUND UNIVERSITY (SE)

09.45 Explorations of Optimal Core and Cache Placements for Chip Multiprocessor
Thomas Canhao XU et al, University of Turku (FI)

10.05 FPGA Implementation of Decimal Processors for Hardware Acceleration
Nicolas Borup et al, Technical University of Denmark (DK)

6. Poster Session II
10.25 Coffee / Poster session:

Architecture-level analysis and evaluation of transient errors on NoC
Jiajia Jiao et al, Shanghai Jiao Tong University (CN)

7.1 Wireless Receivers
CHAIR: JAN MIKKELSEN, AALBORG UNIVERSITY (DK)

11.00 Highly Reliable and Power Efficient NOC Interconnects
Deena M.Zamzam et al, German University in Cairo (EG)

11.30 Yield modeling and Yield-aware Mapping for Application Specific Networks-on-Chip
Seyed Hassan Khalilinezhad et al, Islamic Azad University (IR)

11.50 A Low-Cost Processing Element Recovery Mechanism for Fault Tolerant Networks-on-Chip
Khalid Lattif et al, University of Turku (FI)

7.2 Design Methodologies
CHAIR: PETER NILSSON, LUND UNIVERSITY (SE)

11.10 A GALS ASIC Implementation from a CAL Dataflow Description
Hemanth Prabhu et al, Lund University (SE)

11.30 Temperature Dependent Wire Delay Estimation in Floorplanning
Wei Liu et al, Politecnico di Torino (IT)

11.50 Initial Version of Matlab/Simulink Based Tool for VHDL Code Generation and FPGA Implementation of Elementary Generalized Unitary Rotation
Gatis Valters, Riga Technical University (LV)

12.10 Lunch

13.10 Invited talk: A new digital signal processing approach
Lars Risbo, Texas Instruments Denmark (DK)

8.1 Phase Locked Loops
CHAIR: HENRIK SJÖLAND, LUND UNIVERSITY (SE)

13.55 A 2.7GHz Divider-less All Digital Phase-Locked Loop with 625Hz Frequency Resolution in 90nm CMOS
Mohammed Abdulaziz et al, Lund University (SE)

14.15 A 0.13µm CMOS ΔΣ PLL FM Transmitter
Ying Wu et al, Lund University (SE)
14.35 A Digital PLL with a Multi-Delay Coarse-Fine TDC
Ying Wu et al, Lund University (SE)

14.55 A novel approach of Cap-sharing to reduce the big loop filter capacitance in semi-digital PLL
Puneet Sareen et al, Texas Instruments (DE)

8.2 LOW POWER TECHNIQUES
CHAIR: KJELL JEPPSON, CHALMERS UNIVERSITY OF TECHNOLOGY (SE)

13.55 Measurement of a System-Adaptive Error-Detection Sequential Circuit with Subthreshold SCL
Matthew Turnquist et al, Aalto University (FI)

14.15 A Novel Low-Energy Match Line Sensing Scheme for Ternary Content Addressable Memory Using Charge Sharing
Syed Iftekhar Ali et al, Islamic University of Technology (BD)

14.35 Impact of Switching Activity on the Energy Minimum Voltage for 65 nm Sub-VT CMOS
Oskar Andersson et al, Lund University (SE)

14.55 Low Power Programmable Frequency Divider for IEEE 802.15.4a Standard
Denys Martynenko et al, IHP (DE)

15.15 Closing remarks and NORCHIP 2012

SESSION ORGANISATION
Both oral and poster presentations have been carefully selected through a regular review process and they will all appear in the proceedings. Equal quality measures have been applied to posters and lectures. Papers for oral presentation are selected based on thematic composition of sessions.

PROCEEDINGS
USB stick proceedings of the conference contributions will be distributed upon registration. Each participant will receive a copy of the proceedings. Proceedings and all presentations will be in English.

BEST ANALOG PAPERS
The Management Committee has since 1992 made special issues of the Springer International Journal on Analog Integrated Circuits and Signal Processing. Also this year we will publish a number of the best analog papers in the journal.
http://www.springer.com/engineering/circuits+%26+syste ms/journal/10470

BEST DIGITAL PAPERS
The best digital papers will be invited to publish in the international Elsevier journal Embedded Hardware Design (MICPRO).
http://www.elsevier.com/wps/find/journaldescription.cws _home/525449/description#description

GENERAL SCOPE OF THE CONFERENCE
The NORCHIP conference is the main microelectronics event of the Nordic countries. The annual IEEE CAS sponsored conference covers all areas of microelectronics, spanning from large digital systems to simple analog circuits. The wide scope of NORCHIP is intentional promoting cross-field collaboration.

NORCHIP is a well established conference with representation from both academia and industry. Papers of the highest scientific and technical quality are presented together with selected invited speakers and pre-conference tutorial sessions.

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CONFERENCE VENUE / ACCOMMODATION
The conference location is in the heart of Lund at:

Grand Hotel
Bantorget 1
SE-221 04 Lund
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www.grandilund.se
Tel.: +46 46 280 6100, E-mail: hotel@grandilund.se

Accommodation can be booked at the registration form.

REGISTRATION
The registration form on www.norchip.org must be completed and returned to the Conference Secretariat, together with full payment. The registration fee of EUR 450 includes proceedings, banquette dinner, lunches and coffee breaks. The fee for the tutorial is charged separately. Registration deadline is 31 October. Registrations are acknowledged upon reception.

PRE-CONFERENCE TUTORIALS
Two pre-conference tutorials are offered on Sunday afternoon:

Integrated voltage-controlled oscillators (VCOs)
By Pietro Andreani, Lund University (SE)

DSP Architecture Optimization
By Dejan Marković, University of California LA (USA)